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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/703,845	11/02/2000	Matsumoto Toshiyuki	18940/36899	2544

23646 7590 05/25/2004

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EXAMINER	
NGUYEN, TUNG X	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 05/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/703,845	TOSHIYUKI ET AL.	
	Examiner	Art Unit	
	Tung X Nguyen	2829	

-- Th MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-22* is/are allowed.

6)☒ Claim(s) *1,2,6,7,9 and 10* is/are rejected.

7)☒ Claim(s) *3-5,8 and 11-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "plurality of third terminals" recited in claim 2 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is unclear that "*plurality of third terminals* each separated from the first terminal by an insulator", is it shown in any drawings?

To apply art, examiner assumes that plurality of third terminals is the same with the rail terminal for applying the signals.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1-2, 6-7, 9, 10, are rejected under 35 U.S.C. 102(a) as being anticipated by Tao (u.s.p 6,456,105).

As to claim 1, Tao discloses in Fig. 1, a method of measuring capacitance of micro structures of an integrated circuit (10), wherein the micro structure having a first terminal (18) and a second terminal (12) separated by an insulator (14) and the integrated circuit included at least a third terminal (20) separated from the first terminal (18) by an insulator (16), the method comprising steps of: applying a biasing potential (Vg) to the second terminal; applying a common potential (GND of figure 1) to the first and third terminals; and measuring the first capacitance (col. 1, lines 60-67), so determine the gate oxide layer (14) considered the electrical thickness (Tox) between the gate (12) and source/drain terminal. Therefore, Tao disclose the step of measuring an electrical characteristic between the first and second terminal to determine the capacitance between the first and second terminals (col. 1, line 60-67; and col. 2, lines 45-67).

As to claim 2, Tao discloses in Fig. 1, wherein integrated circuit with a rail terminal (20) separated from the first terminal (18) by an insulator (16); and applying the common potential to the first terminal and the third terminal (GND).

As to claim 6, Tao discloses in Fig. 1, the measurement is taken at the first terminal (12, and col. 1, line 60-67; and col. 2, lines 45-67).

As to claim 7, Tao discloses in Fig. 1, the steps of applying a biasing potential (Vg) to one of the source (20) or drain (18); applying a common potential (GND of figure 1) to the gate terminals, connected to the first terminal (18) to the source or drain (20); and measuring the first capacitance (col. 1, lines 60-67), so determine the gate oxide layer (14) considered the electrical thickness (Tox) between the gate (12) and source/drain terminal (18, 20). Therefore, Tao disclose the step of measuring an electrical characteristic between the gate terminal and the source/drain terminals to determine the capacitance between the gate and source/drain terminals (col. 1, line 60-67; and col. 2, lines 45-67) (and also regarding to claim 9).

As to claim 10, Tao discloses in Fig. 1, the microstructure is a field effect transistor (10) having a gate (12), and a source (18) and a drain (20) having a PN junction with a body (16); and the capacitance of the PN junction between one terminal to another (12, 18, 20, 16) by steps of: applying a biasing potential (Vg) to the body connected to the second terminal (12); applying a common potential (GND of figure 1) to one of source and drain (18, 20) connected to the first terminal (18), and the other of the source (18) and the drain (20) connected to the third terminal (20); and measuring an electrical characteristic between the one of the source or drain terminals to the body to determine the capacitance between the one of the source or drain terminals to the body (col. 1, line 60-67; and col. 2, lines 45-67).

Allowable Subject Matter

6. Claims 20-22 are allowed.

7. Claims 3-5, and 8, 11-16, 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As to claims 3-5, and 8, the prior art does not disclose the steps of measuring the electrical characteristic between the gate and the source and the *drain to determine the sum of the capacitance between the gate and the source and the drain.*

As to claims 11-16, 22, the prior art does not teach or suggest the steps of measuring the electrical characteristic between the word or bit line and the neighbor word or bit line to determine the capacitance between the word or bit line and its neighbor word or bit line; In combination with the other claimed features.

As to claims 17-19, the prior art does not teach or suggest the integrated circuit includes a plurality of conductors separated by insulators; and measuring the electrical characteristic between the conductor and the one neighbor conductor to determine the capacitance between the conductor and the one neighbor conductor.

As to claims 20-21, the prior art does not disclose the steps of: applying a common potential to gate, and the other of the source or drain if the biasing potential is applied to the one of the source or drain, and the common potential to one of the one of the source or drain, the other of the source or drain and the channel area if the biasing potential is applied to the gate; in combination with the other claimed features.

Response to Arguments

8. Applicant's arguments, see "Remark", filed 03/05/04, with respect to claims 1-22 have been fully considered and are persuasive. The rejection of claims number 1-10, 17-21 has been withdrawn.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung X Nguyen whose telephone number is (571) 272-1967. The examiner can normally be reached on 8:30am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TN
5/10/04

David A. Zarneke
Primary Exmr
5/13/04